M. Tech. - COURSE STRUCTURE & SYLLABUS – RK24

(Applicable from the academic year 2024-25 onwards)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE STRUCTURE & SYLLABUS

M. Tech (VLSI and Embedded System Design) Programme

Course Code Format:

Regulation	Branch	Year	Semester	Course Serial Number
2 Digits	2 Digits	1 Digit	1 Digit	2 Digits
24	68	1/2	1/2	01/02/03/04/..../09/10

Branch Code:

Code	Branch	Specialization
68	Electronics and Communication Engineering	VLSI and Embedded System Design

Chairman - BoS
Electronics & Communication Engineering
RKCE (Autonomous)

M. Tech I Year, I Semester (VLSI and Embedded System Design)

S.No.	Course Code	Category	Title	L	T	P	Credits
1	24681101	Core	RTL Simulation and Synthesis with PLDs	3	0	--	3
2	24681102	Core	Microcontrollers and Programmable Digital Signal Processors	3	0	--	3
3	24681103	Elective-I	• Digital Signal and Image Processing • Parallel Processing • VLSI signal processing	3	0	--	3
4	24681104	Elective-II	• Programming Languages for Embedded Systems • System Design with Embedded Linux • CAD of Digital System	3	0	--	3
5	24681105		Research Methodology & IPR	2	0	0	2
6	24681106	Lab	RTL Simulation and Synthesis with PLDs Lab	--	--	4	2
7	24681107	Lab	Microcontrollers and Programmable Digital Signal Processors Lab	--	--	4	2
8	24681108	Audit	Audit Course –1	2	0	0	0
Total				16	0	8	18

M. Tech I Year, II Semester (VLSI and Embedded System Design)

S.No.	Course Code	Category	Title	L	T	P	Credits
1	24681201	Core	Analog and Digital CMOS VLSI Design	3	0	--	3
2	24681202	Core	Real Time Operating Systems	3	0	--	3
3	24681203	Elective-III	• Memory Architectures • SoC Design • Low power VLSI Design	3	0	--	3
4	24681204	Elective-IV	• Communication Buses and Interfaces • Network Security and Cryptography • Physical design automation	3	0	--	3
5	24681205	Lab	Analog and Digital CMOS VLSI Design Lab	--	--	4	2
6	24681206	Lab	Real Time Operating Systems Lab	--	--	4	2
7	24681207	Project	Mini Project With Seminar	--	--	4	2
8	24681208	Audit	Audit Course –2	2	0	0	0
Total				14	0	12	18

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

M. Tech II Year, I Semester (VLSI and Embedded System Design)

S.No.	Course Code	Category	Title	L	T	P	Credits
1	24682101	Elective-V	• IOT and its Applications • Hardware Software co-design • Artificial Intelligence	3	0	--	3
2	24682102	Open Elective	• Business Analytics • Industrial Safety • Operations Research • Cost Management of Engineering Projects • Composite Materials • Waste to Energy	3	0	--	3
3	24682103	Project	Dissertation Phase-I / Industrial Project (To be continued and Evaluated next Semester)*	--	--	20	10
Total				6	0	20	16

* Evaluated and displayed in 4th Semester marks list
** Students Going for Industrial Project / Thesis will complete these courses through MOOCS

M. Tech II Year, II Semester (Specialisation Name)

S.No.	Course Code	Category	Title	L	T	P	Credits
1	24682201	Project	Project / Dissertation Phase II (Continued from III Semester)	0	0	32	16
Total				0	0	32	16

Audit course 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills.

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RTL Simulation and Synthesis with PLDs

Course Objectives:

- To introduce Verilog HDL for the design and functionality verification of a digital circuit.
- To understand the design of data path and control circuits for sequential machines
- To introduce the concept of realizing a digital circuit using PLDs

UNIT-I:

Verilog HDL: Importance of HDLs, Lexical Conventions of Verilog HDLGate level modeling: Built in primitive gates, switches, gate delays Data flow modeling: Continuous and implicit continuous assignment, delays Behavioural modeling: Procedural constructs, Control and repetition Statements, delays, function and tasks.

UNIT-II:

Digital Design: Design of BCD Adder, State graphs for control circuits, shift and add multiplier, Binary divider.FSM and SM Charts: Finite state diagram, Implementation of sequence detector using FSM, State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

UNIT-III:

ASIC Design Flow: Simulation, simulation types, Synthesis, synthesis methodologies, translation, mapping, optimization, Floor planning, Placement, routing, Clock tree synthesis, Physical verification.

UNIT-IV:

Static Timing Analysis: Timing paths, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs, setup and hold time Violations, steps to remove Setup and hold time violations.

UNIT-V:

Digital Design using PLD"s: ROM, PLA, PAL- Registered PAL"s, Configurable PAL"s, GAL. CPLDs: Features, programming and applications using complex programmable logic devices. FPGAs: Field Programmable gate arrays Logic blocks, routing architecture, design flow.

TEXT BOOKS:

1. Verilog HDL,A Guide to Digital Design and Synthesis Samir Palnitkar, 2nd Edition, 2003
2. Fundamentals of Logic Design, Charles H. Roth, 5th Edition. Cengage Learning, 2010.
3. Verilog HDL Synthesis A Practical Primer by Bhasker J, 1st edition, 1998
4. Modern Digital Electronics P Jain, 3rd Edition, TMH, 2003.
5. Data Sheets for CPLD & FPGA architectures, 1996.

REFERENCES:

1. Donald D Givone, "Digital principles and Design", TMH, 2016
2. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books, 2002.
3. Richard S. Sandige, "Modern Digital Design", MGH, International Editions, 1990

Course Outcomes:

After completing this course the student will be able to

- Develop the Verilog HDL to design a digital circuit.
- Appreciate the analysis of finite state machine of a controlling circuit
- Understand the Static Timing Analysis and clock issues in digital circuits
- Verify the functionality of the digital designs using PLDs.

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Microcontrollers and Programmable Digital Signal Processors

Course Objectives:

- To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
- To be able to identify and characterize architecture of Programmable DSP Processors
- To develop small applications by utilizing the ARM processor core and DSP processor based platform.

Unit 1: ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

Unit 2: Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

Unit 3: LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

Unit 4: Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

Unit 5: VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing

Text Books:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programmingand Applications" , TMH , 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide:Designing and Optimizing", Morgan Kaufman Publication

Reference Books:

1. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
3. Technical references and user manuals on www.arm.com.

Course Outcomes:

At the end of this course, students will be able to

- Compare and select ARM processor core based SoC with several features/peripheralsbased on requirements of embedded applications.
- Identify and characterize architecture of Programmable DSP Processors
- Develop small applications by utilizing the ARM processor core and DSP processor based platform.

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Digital Signal and Image Processing
(Elective I)

UNIT I

Review of Discrete Time signals and systems, Characterization in time, Z and Fourier domain, FastFourier Transform using Decimation In Time (DIT) and Decimation In Frequency (DIF) Algorithms.

UNIT II

IIR Digital Filters: Introduction, Analog filter approximations – Butterworth and Chebyshev, Design of IIR Digital filters from analog filters using Impulse Invariance, Bilinear Transformation methods.
FIR Digital Filters: Introduction, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters.

UNIT III

Analysis Of Finite Word length Effects: The Quantization Process and Errors, Quantization of Fixed-Point Numbers, Quantization of Floating-Point Numbers, Analysis of Coefficient Quantization effects.
Introduction To Digital Image Processing: Introduction, components in image processing system, Applications of Digital image processing, Image sensing and acquisition, Image sampling, Quantization, Basic Relationships between pixels, Image Transforms: 2D-DFT, DCT, Haar Transform.

UNIT IV

Image Enhancement: Intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, the basics of filtering in the frequency domain, image smoothing using frequency domain filters, Image Sharpening using frequency domain filters, Selective filtering.
Image Restoration: Introduction, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.
Image Segmentation: Fundamentals, point, line, edge detection, thresholding, region based segmentation.

UNIT V

Image Compression: Fundamentals, Basic compression methods: Huffman coding, Arithmetic coding, Run-Length coding, Block Transform coding, Predictive coding, Wavelet coding.
Color Image Processing: color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation basedon color, noise in color images, color image compression.

Text Books:

1. Digital Signal Processing, Principles, Algorithms, and Applications: John G. Proakis, Dimitris G.Manolakis,PearsonEducation/PHI,2007.
2. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition,2006
3. Rafael C.Gonzalez and Richard E. Woods, "Digital Image Processing", Pearson Education, 2011.
4. S.Jayaraman, S.Esakkirajan, T.Veerakumar, "Digital Image Processing", Mc Graw Hill Publishers,2009

Reference Books:

1. Digital Signal Processing: Andreas Antoniou, TATA McGraw Hill , 2006
2. Digital Signal Processing: MH Hayes, Schaum"s Outlines, TATA Mc-Graw Hill, 2007.
3. Anil K. Jain, "Fundamentals of Digital Image Processing," Prentice Hall of India, 2012.

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Course Outcomes:

At the end of this course, students will be able to

- Analyze discrete-time signals and systems in various domains (i.e Time, Z and Fourier)
- Design the digital filters (both IIR and FIR) from the given specifications
- Analyze the quantization effects in digital filters and understand the basics of image sampling, quantization and image transforms.
- Understand the concepts of image enhancement, image restoration and image segmentation.
- Know the various methods involved in image compression and fundamentals in color image processing.

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Parallel Processing
(Elective I)

Unit 1: Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

Unit 2: Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

Unit 3: VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

Unit 4: Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

Unit 5: Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

Text Books:

1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
2. Kai Hwang, "Advanced Computer Architecture", TMH
3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.

Reference Books:

1. William Stallings, "Computer Organization and Architecture, Designing for performance "Prentice Hall, Sixth edition
2. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing", MGH
3. David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan

Course Outcomes:

At the end of this course, students will be able to

- Identify limitations of different architectures of computer
- Analysis quantitatively the performance parameters for different architectures
- Investigate issues related to compilers and instruction set based on type of architectures.

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VLSI Signal Processing
(Elective I)

UNIT -I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing

Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT –II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems

Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

Unit V: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.
Numerical strength reduction, synchronous, wave and asynchronous pipe lines, lowpower design.
Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Text Books:

1. Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and implementation[A2] , Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall,1985.

Course Outcomes

On successful completion of the module, students will be able to:

- Ability to modify the existing or new DSP architectures suitable for VLSI.
- Understand the concepts of folding and unfolding algorithms and applications.
- Ability to implement fast convolution algorithms.
- Low power design aspects of processors for signal processing and wireless applications.

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Programming Languages for Embedded Systems
(Elective II)

Unit 1: Embedded „C" Programming Bitwise operations, Dynamic memory allocation, OS services. Linked stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Embedded Software Development Cycle and Methods (Waterfall, Agile)

Unit 2: Object Oriented Programming Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

Unit 3: CPP Programming: „cin", „cout", formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, „this" pointer, constructors, destructors, friend function, dynamic memory allocation

Unit 4: Overloading and Inheritance: Need of operator overloading, overloading the assignment, Overloading using friends, type conversions, single inheritance, base and derived classes, friend Classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, Polymorphism, virtual functions.

Unit 5: Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.
Scripting Languages:
Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

Text Books:
1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O"Reilly Publications, 6th Edition 2011

Reference Books:
1. Michael Berman, "Data structures via C++", Oxford University Press, 2002
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey& Sons, 2005Kaufmann.

Course Outcomes:
At the end of this course, students will be able to
- Write an embedded C application of moderate complexity.
- Develop and analyze algorithms in C++.
- Differentiate interpreted languages from compiled languages.

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System Design with Embedded Linux
(Elective II)

Course Objectives:

- To understand the embedded Linux development model.
- To be able to write and debug applications and drivers in embedded Linux.
- To be able to understand and create Linux BSP for a hardware platform

Unit 1:
Embedded Linux , Vendor Independence, Time to Market,Varied Hardware Support, Open Source, Standards (POSIX®) Compliance, Embedded Linux Versus Desktop Linux, Embedded Linux Distributions, BlueCat Linux, Cadenux , Denx, Embedded Debian (Emdebian),ELinOS (SYSGO), Metrowerks ,MontaVista Linux, RTLinuxPro, TimeSys Linux.

Unit 2: Embedded Linux Architecture, Real-Time Executive, Monolithic Kernels, MicrokernelKernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence, Boot Loader Phase, Kernel Start-Up, User Space Initialization.

Unit 3: Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules.

Unit 4: Porting Applications, Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver, Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

Unit 5: Building and Debugging: Kernel, Building the Kernel, Building Applications, Building the Root File System, Integrated Development Environment, Debugging Virtual Memory Problems , Kernel Debuggers, Root file system Embedded Graphics. Graphics System, Linux Desktop Graphics, Embedded Linux Graphics, Embedded Linux Graphics Driver, Windowing Environments, Toolkits, and Applications,Case study of uClinux

Text Books:

1. KarimYaghmour, "Building Embededd Linux Systems", O'Reilly & Associates
2. P Raghvan, Amol Lad, SriramNeelakandan, "Embedded Linux System Design and Development", Auerbach Publications

Reference Books:

1. Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach",Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building withEmbedded Linux", Wiley, 1st Edition, 2014.

Course Outcomes:

At the end of this course, students will be able to

- Get the familiarity about embedded Linux development model.
- Write and debug applications and drivers in embedded Linux.
- Understand and create Linux BSP for a hardware platform

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CAD of Digital System
(Elective II)

Course Objectives

- To understand the fundamentals of CAD tools for modeling, design, test and verification of VLSI systems
- To study various phases of CAD, including simulation, physical design, test andVerification.
- To be able to demonstrate the knowledge of computational algorithms and tools for CAD.

Unit 1: Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules Layout of Basic Devices, Fabrication Process and its Impact on Physical Design, Scaling Methods , Status of Fabrication Process, Issues related to the Fabrication Process, Future of Fabrication Process , Solutions for Interconnect Issues, Tools for Process Development

Unit 2: VLSI design automation tools – Data Structures and Basic Algorithms, Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, graph theory and Computational complexity, tractable and intractable problems.

Unit 3: General purpose methods for combinational optimization – **Partitioning-** Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms , Simulated Annealing Simulated Evolution, Other Partitioning Algorithms Performance Driven Partitioning **Floor planning-** Chip planning , Pin Assignment , Integrated Approach, **Placement-** Problem Formulation , Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms , Performance Driven Placement, **Routing** -Global Routing, , Problem Formulation , Classification of Global Routing Algorithms, Maze Routing Algorithms , Line-Probe Algorithms, Shortest Path Based Algorithms. Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing

Unit 4: Simulation- Gate-level Modeling and Simulation, Switch-level Modeling and Simulation, **Logic Synthesis and Verification -** Introduction to Combinational Logic Synthesis, Binary-decision Diagrams, Two-level Logic Synthesis, **High-level Synthesis-** Hardware Models for High level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling

Unit 5: MCMs-VHDL-Verilog-implementation of simple circuits using VHDL

Text Books:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".
2. S.H. Gerez, "Algorithms for VLSI Design Automation.

Course Outcomes:

At the end of this course, students will be able to

- Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
- Understand various phases of CAD, including simulation, physical design, test andverification.
- Demonstrate knowledge of computational algorithms and tools for CAD.

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Research Methodology and IPR

Unit 1: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit 2: Effective literature studies approaches, analysis Plagiarism, Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit 3: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 4: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patentinformation and databases. Geographical Indications.

Unit 5: New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies,IPR and IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science& engineering students""
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.

Reference Books:

1. Mayall , "Industrial Design", McGraw Hill, 1992.
2. Niebel , "Product Design", McGraw Hill, 1974.
3. Asimov , "Introduction to Design", Prentice Hall, 1962.
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New
5. Technological Age", 2016.
6. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

Course Outcomes:

At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation,it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about,economic growth and social benefits.

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RTL Simulation and Synthesis with PLDs Lab

List of Experiments:

1. Verilog implementation of
   - 8:1 Mux/Demux,
   - Full Adder, 8-bit Magnitude comparator,
   - 3-bit Synchronous Counters
   - Parity generator.
2. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3. Vending machines - Traffic Light controller, ATM, elevator control.
4. PCI Bus & arbiter and downloading on FPGA.
5. UART/ USART implementation in Verilog.
6. Realization of single port SRAM in Verilog.
7. Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
8. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Identify, formulate, solve and implement problems in signal processing, communicationSystems etc using RTL design tools.
- Use EDA tools like Cadence, Mentor Graphics and Xilinx.

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Microcontrollers and Programmable Digital Signal Processors Lab

List of Assignments:

Part A

Experiments to be carried out on Cortex-M3 development boards and using GNUTool chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B

Experiments to be carried out on DSP C6713 evaluation kits and using Code ComposerStudio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Install, configure and utilize tool sets for developing applications based on ARM processor Core SoC and DSP processor.
- Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

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Analog and Digital CMOS VLSI Design

Course objectives:

- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Combinational MOS logic circuits, and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories whichare the basics for the design of high performance digital integrated circuits.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

Syllabus Contents:

Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process

Digital CMOS Design:

Unit 1: Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their Evaluation, Dynamic behavior, Power consumption.

Unit 2: Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.
Combinational logic: Static CMOS design, Logic effort, Rationed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Unit 3: Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches,
Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design:

Unit 4: Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate
stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

Unit 5: Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise. Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP

Text Books:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.

Reference Books:

1. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.

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2. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
3. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",TMH, 3rdEdition.
4. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Course Outcomes:

At the end of this course, students will be able to

- Appreciate the trade-offs involved in analog integrated circuit design.
- Understand and appreciate the importance of noise and distortion in analog circuits.
- Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
- Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.
- Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.

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REAL TIME OPERATING SYSTEMS

Course Objectives:

- To Know the Basic Designs using an RTOS.
- To Know the Functions and Types of RTOS for Embedded Systems.
- To Analyze the issues in real time operating systems
- To Study the Programming Concepts of RT Linux.
- To Understand Applications Control by RT Linux System.
- To Analyze the Operating System Software

UNIT I

Introduction to Real-Time Operating Systems - Defining an RTOS, The scheduler, Kernel Objects and services, Key characteristics of an RTOS

Task- Defining a Task, Task States and Scheduling, Typical Task Operations, Typical Task Structure, Synchronization, Communication and Concurrency

UNIT II

Semaphores - Defining Semaphores, Typical Semaphore Operations, Typical Semaphore Use

Message Queues - Defining Message Queues, Message Queue States, Message Queue Content, Message Queue Storage, Typical Message Queue Operations, Typical Message Queue Use, Pipes, Event Registers, Signals and condition Variables

UNIT III

Exceptions and Interrupts - Exceptions and Interrupts, Applications of Exceptions and Interrupts, Closer look at exceptions and interrupts, processing general Exceptions, Nature of Spurious Interrupts

Timer and Timer Services - Real-Time clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routines.

I/O Subsystems - I/O concepts, I/O subsystems

UNIT IV

Memory Management - Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory management in Embedded Systems, Blocking VS. Non-Blocking Memory Functions, Hardware Memory Management Units

Modularizing an application for concurrency- An outside-in approach to decompose Applications, Guidelines and Recommendations for Identifying Concurrency, Schedulability Analysis

UNIT V

Synchronization and Communication - Synchronization, Communication, Resource Synchronization Methods, Critical section, Common practical design patterns, Specific Solution Design Patterns,

Common Design Problems - Resource Classification, Deadlocks, Priority Inversion.

Text Books

1. Qing Li, Caroline Yao (2003), "Real-Time Concepts for Embedded Systems", CMP Books.

Course Outcomes

Upon the completion of the course student will be able to

- Illustrate real time programming concepts.
- Apply RTOS functions to implement embedded applications
- Understand fundamentals of design consideration for embedded applications

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Memory Architectures
(Elective III)

Unit 1: Random Access Memory Technologies:
Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

Unit 2:DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

Unit 3: Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit 4: Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Unit 5 : Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues,

Text Books:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Inter science
2. Kiyooltoh, "VLSI memory chip design", Springer International Edition

Reference Books:

1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability , PHI

Course Outcomes:

At the end of the course, students will be able to:

- Select architecture and design semiconductor memory circuits and subsystems.
- Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
- Know how the state-of-the-art memory chip design

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SoC Design (Elective III)

Unit 1: ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Unit 2: NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction setProcessors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Unit 3: Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clocktree design issues.

Unit 4:Low power SoC design / Digital system: Design synergy, Low power system perspective- power gating, clock gating, adaptive voltagescaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit 5 :Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trailspaths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs.

Text Books:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

Reference Books:

1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center,2000
2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley

Course Outcomes:

At the end of the course, students will be able to:

- Identify and formulate a given problem in the framework of SoC based design approaches DesignSoC based system for engineering applications
- Realize impact of SoC on electronic design philosophy and Macro-electronics thereby
- incline towards entrepreneurship & skill development.

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Low Power VLSI Design
(Elective III)

Unit 1: Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree Of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd& Vt on speed, constraints on Vt reduction, transistor sizing& optimal gate oxide thickness, impact of technology scaling, technology innovations.

Unit 2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network.

Unit 4: Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers.

Unit 5: Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits,
low power SRAM circuits. Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power.

Text Books:

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic,2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sonsInc.,2000.

Reference Books:

1. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design",Kluwer,1995
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

Course Outcomes:

At the end of the course, students will be able to:

- Identify the sources of power dissipation in digital IC systems & understand theimpact of power on system performance and reliability.
- Characterize and model power consumption & understand the basic analysismethods.
- Understand leakage sources and reduction techniques

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Communication Busses and Interfaces
(Elective IV)

UNIT I
Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features Limitations and applications of RS232, RS485, I^2C , SPI

UNIT IICAN
ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT IIIPCIe
Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT IVUSB
Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor,String descriptor. Device driver.

UNIT V
Data streaming Serial Communication Protocal- Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

TEXTBOOKS
1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,

REFERENCES
1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

Course Outcomes:
At the end of the course, students will be able to:
- Select a particular serial bus suitable for a particular application.
- Develop APIs for configuration, reading and writing data onto serial bus.
- Design and develop peripherals that can be interfaced to desired serial bus.

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Network Security and Cryptography (Elective IV)

Unit 1: Security & Number Theory
Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysisof Classical Encryption Techniques. Introduction, Fermat"s and Euler"s Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Unit 2: Private-Key (Symmetric) Cryptography
Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES),Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Unit 3: Public-Key (Asymmetric) Cryptography
RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

Unit 4: Authentication
IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure ElectronicTransaction.

Unit 5: System Security
Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, VirusCountermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

Text Books:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communicationin a Public World", Prentice Hall, 2nd Edition

Reference Books:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

Course Outcomes:
At the end of the course, students will be able to:

- Identify and utilize different forms of cryptography techniques.
- Incorporate authentication and security in the network applications.
- Distinguish among different types of threats to the system and handle the same.

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Physical Design Automation
(Elective IV)

UNIT -I

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNIT -II:

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms

UNIT -III:

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

UNIT -IV:

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum colouring, maximum k-independent set algorithm, algorithms for circle graphs.

UNIT -V:

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

Course Outcomes:

At the end of the course, students will be able to:

- Understand the relationship between design automation algorithms and Various constraints posedby VLSI fabrication and design technology.
- Adapt the design algorithms to meet the critical design parameters.
- Identify layout optimization techniques and map them to the algorithms
- Develop proto-type EDA tool and test its efficacy

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Analog and Digital CMOS VLSI Design Lab

The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology with Mentor Graphics Tool/Cadence/ Synopsys/Industry Equivalent Standard Software.

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. simple current mirror
6. cascode current mirror.
7. Wilson current mirror.
8. Full Adder
9. RS-Latch
10. Clock Divider
11. JK-Flip Flop
12. Synchronous Counter
13. Asynchronous Counter
14. Static RAM Cell

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Real Time Operating Systems Lab

- The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM- Cortex.
- The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.
- The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.

List of Experiments:

Part-I: Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER"S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader"s Writer"s Problem for concurrent Tasks.

Part-II: Experiments on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communicationwith PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC"s.

Lab Requirements:

Software:

- Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
- LINUX Environment for the compilation using Eclipse IDE & Java with latestversion.

Hardware:

- The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
- Serial Cables, Network Cables and recommended power supply for the board.

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MINI PROJECT

Syllabus Contents

The students are required to search / gather the material / information on a specific a topic comprehend it and present / discuss in the class.

Course Outcomes

At the end of this course, students will be able to

- Understand of contemporary / emerging technology for various processes and systems.
- Share knowledge effectively in oral and written form and formulate documents

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AUDIT 1 and 2: ENGLISH FOR RESEARCH PAPER WRITING

Course objectives:

Students will be able to:

- Understand that how to improve your writing skills and level of readability Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Syllabus

Units	CONTENTS	Hours
1	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	4
2	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction	4
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	4
4	key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,	4
5	skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	4
6	useful phrases, how to ensure paper is as good as it could possibly be the first- time submission	4

Suggested Studies:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman"sbook .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

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AUDIT 1 and 2: DISASTER MANAGEMENT

Course Objectives: -Students will be able to:

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches,
- planning and programming in different countries, particularly their home country or the countries they work in

Syllabus

Units	CONTENTS	Hours
1	**Introduction** Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.	4
2	**Repercussions Of Disasters And Hazards:** Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man- made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	4
3	**Disaster Prone Areas In India** Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics	4
4	**Disaster Preparedness And Management** Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.	4
5	**Risk Assessment** Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People"s Participation In Risk Assessment. Strategies for Survival.	4
6	**Disaster Mitigation** Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.	4

Suggested Readings:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies ""New Royal book Company.
2. Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., New Delhi.

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AUDIT 1 and 2: SANSKRIT FOR TECHNICAL KNOWLEDGE

Course Objectives

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjectsenhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Unit	Content	Hours
1	• Alphabets in Sanskrit, • Past/Present/Future Tense, • Simple Sentences	8
2	• Order • Introduction of roots • Technical information about Sanskrit Literature	8
3	• Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	8

Suggested reading

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India"s Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Output

Students will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood Being a logical language will help to develop logic in

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AUDIT 1 and 2: SANSKRIT FOR TECHNICAL KNOWLEDGE

Course Objectives

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjectsenhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Syllabus

Unit	Content	Hours
1	• Alphabets in Sanskrit, • Past/Present/Future Tense, • Simple Sentences	8
2	• Order • Introduction of roots • Technical information about Sanskrit Literature	8
3	• Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	8

Suggested reading

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India"s Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Output

Students will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

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AUDIT 1 and 2: VALUE EDUCATION

Course Objectives

Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Syllabus

Unit	Content	Hours
1	• Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. • Moral and non- moral valuation. Standards and principles. • Value judgements	4
2	• Importance of cultivation of values. • Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism.Love for nature ,Discipline	6
3	• Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. • Punctuality, Love and Kindness. • Avoid fault Thinking. • Free from anger, Dignity of labour. • Universal brotherhood and religious tolerance. • True friendship. • Happiness Vs suffering, love for truth. • Aware of self-destructive habits. • Association and Cooperation. • Doing best for saving nature	6
4	• Character and Competence –Holy books vs Blind faith. • Self-management and Good health. • Science of reincarnation. • Equality, Nonviolence ,Humility, Role of Women. • All religions and same message. • Mind your Mind, Self-control. • Honesty, Studying effectively	6

Suggested reading

1 Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

Course outcomes

Students will be able to

1. 1.Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

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AUDIT 1 and 2: CONSTITUTION OF INDIA

Course Objectives:

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals" constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin 1917 and its impact on the initial drafting of the Indian Constitution.

Syllabus		
Units	**Content**	**Hours**
1	• **History of Making of the Indian Constitution:** History Drafting Committee, (Composition & Working)	4
2	• **Philosophy of the Indian Constitution:** Preamble Salient Features	4
3	• **Contours of Constitutional Rights & Duties:** • Fundamental Rights • Right to Equality • Right to Freedom • Right against Exploitation • Right to Freedom of Religion • Cultural and Educational Rights • Right to Constitutional Remedies • Directive Principles of State Policy • Fundamental Duties.	4
4	• **Organs of Governance:** • Parliament, Composition ,Qualifications and Disqualifications • Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions	4
5	• **Local Administration:** • District"s Administration head: Role and Importance, • Municipalities: Introduction, Mayor and role of Elected Representative, CE of Municipal Corporation. • Pachayati raj: Introduction, PRI: ZilaPachayat. • Elected officials and their roles, CEO ZilaPachayat: Position and role. • Block level: Organizational Hierarchy (Different departments), • Village level: Role of Elected and Appointed officials, • Importance of grass root democracy	4
6	• **Election Commission:** • Election Commission: Role and Functioning. • Chief Election Commissioner and Election Commissioners. • State Election Commission: Role and Functioning. • Institute and Bodies for the welfare of SC/ST/OBC and women.	4

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Suggested reading

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Outcomes:

Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution inIndia.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

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AUDIT 1 and 2: PEDAGOGY STUDIES

Course Objectives:

Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Syllabus		
Units	Content	Hours
1	• **Introduction and Methodology:** • Aims and rationale, Policy background, Conceptual framework and terminology • Theories of learning, Curriculum, Teacher education. • Conceptual framework, Research questions. • Overview of methodology and Searching.	4
2	• Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. • Curriculum, Teacher education.	2
3	• Evidence on the effectiveness of pedagogical practices • Methodology for the in depth stage: quality assessment of included studies. • How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? • Theory of change. • Strength and nature of the body of evidence for effective pedagogicalpractices. • Pedagogic theory and pedagogical approaches. • Teachers" attitudes and beliefs and Pedagogic strategies.	4
4	• Professional development: alignment with classroom practices and follow-up support • Peer support • Support from the head teacher and the community. • Curriculum and assessment • Barriers to learning: limited resources and large class sizes	4
5	• **Research gaps and future directions** • Research design • Contexts • Pedagogy • Teacher education • Curriculum and assessment • Dissemination and research impact.	2

Suggested reading

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare,31 (2): 245-261.

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2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, „learning to read" campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

Course Outcomes:

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classroomsin developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy.

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AUDIT 1 and 2: STRESS MANAGEMENT BY YOGA

Course Objectives

1. To achieve overall health of body and mind
2. To overcome stress

Syllabus

Unit	Content	Hours
1	• Definitions of Eight parts of yog. (Ashtanga)	8
2	Yam and Niyam. Do`s and Don"t"s in life. i) Ahinsa, satya, astheya, bramhacharya and aparigraha ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan	8
3	• Asan and Pranayam 1. Various yog poses and their benefits for mind & body 2. Regularization of breathing techniques and its effects-Types of pranayam	8

Suggested reading

1. „Yogic Asanas for Group Tarining-Part-I" : Janardan Swami YogabhyasiMandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

Course Outcomes:

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

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AUDIT 1 and 2: PERSONALITY DEVELOPMENT THROUGH LIFEENLIGHTENMENT SKILLS

Course Objectives

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Syllabus

Unit	Content	Hours
1	Neetisatakam-Holistic development of personality • Verses- 19,20,21,22 (wisdom) • Verses- 29,31,32 (pride & heroism) • Verses- 26,28,63,65 (virtue) • Verses- 52,53,59 (dont"s) • Verses- 71,73,75,78 (do"s)	8
2	• Approach to day to day work and duties. • Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48, • Chapter 3-Verses 13, 21, 27, 35, • Chapter 6-Verses 5,13,17, 23, 35, • Chapter 18-Verses 45, 46, 48.	8
3	• Statements of basic knowledge. • Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 • Chapter 12 -Verses 13, 14, 15, 16,17, 18 • Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42, • Chapter 4-Verses 18, 38,39 • Chapter18 – Verses 37,38,63	8

Suggested reading

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari"s Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya SanskritSansthanam, New Delhi.

Course Outcomes

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality andachieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity Study of Neetishatakam will help in developing versatile personality of students

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